would apply to the case at hand in the following way. Isolation structure x is used in the fabrication of wafer group A, and structure y is used in the fabrication of wafer group B. Then the resulting topography is measured on both sets of wafers. If the resulting topography difference between the two groups is beyond what would be expected with normal random variation, the difference would be considered significant. Obviously, statistical significance can be much more subtle than the first definition above.

Claim Rejections-35 USC § 112

2. The rejection of claims 4 and 5 under 35 U.S.C 112, the first paragraph, in the Non-Final Rejection mailed 03/22/05 is withdrawn. Applicant's admission that such layers are "known to those skilled in the art, and not relevant to the invention" is sufficient to render the limitations anticipated by the prior art regarding the final determination of the patentability.

If by the above comment, the examiner is saying those skilled in the art understand this invention may start with either a bulk semiconductor, or one with epitaxial overlayers, then no response is necessary. If we have misunderstood, we request the examiner clarify the statement.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: [Quotation deleted]

4. Claims 1-5 and 8 are rejected under 35 U.S.C 102(e) as being anticipated by Deshpande et al. (US 2004/0242010 A1).

In re claim 1, Deshpande (esp. Fig 3E) discloses a structure providing anneal cap/ion implant mask (68), and shallow trench isolation (70) features for III-V devices comprising a trench etched into the semiconductor, a combination anneal cap/CMP stop layer, and a dielectric trench fill layer, with significant topography reduction compared to the traditional dielectric structure.

In re claim 1, Deshpande in no way discloses a structure providing anneal cap/ion implant mask (68), and shallow trench isolation (70) features for III-V devices comprising a trench etched into the semiconductor, a combination anneal cap/CMP stop layer, and a dielectric trench fill layer, with significant topography reduction compared to the traditional dielectric structure. To clarify this fact for those not well versed in the art, the following is a step by step description of what would happen when Deshpande's invention was used on GaAs. It will become obvious that the resulting structure has little in common with the current invention.

- Steps leading up to the nitridation step illustrated in Deshpande's Fig. 3D are well known in the art, and are evident in Fig 3D itself.

- Deshpande's Fig. 3D is mostly replicated on the right side of Figure 2 below, One

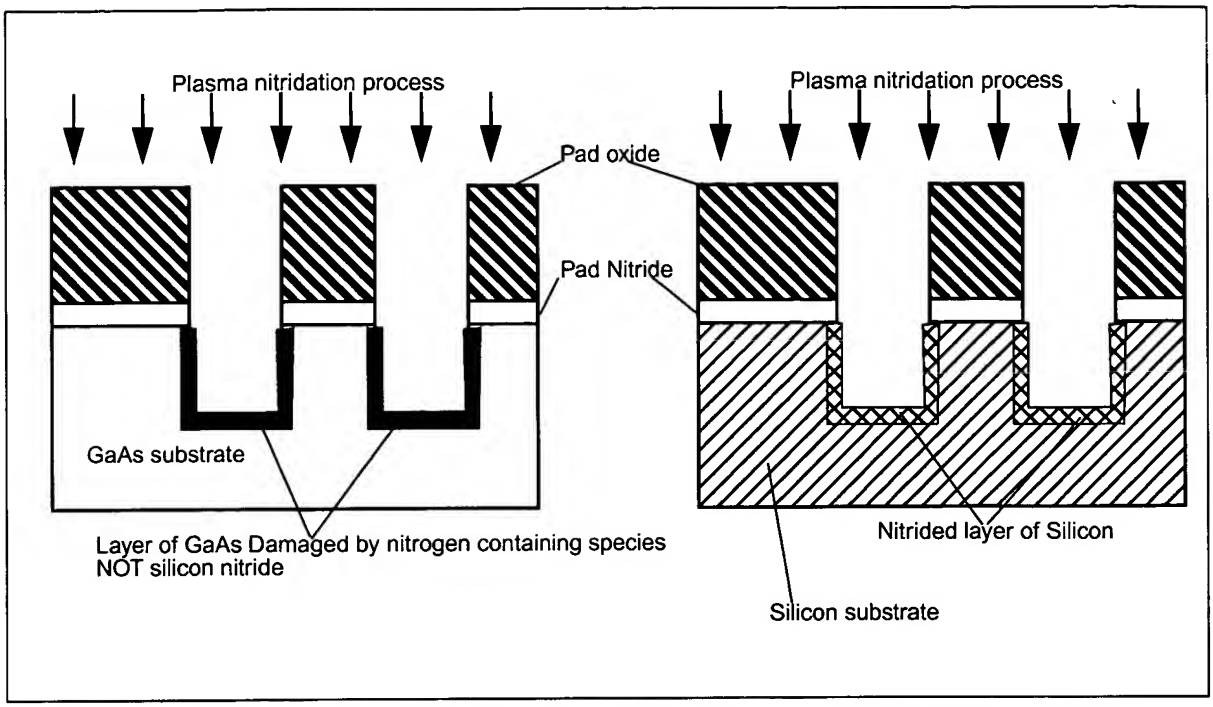

Figure 2: Effects of Deshpande's key process step on GaAs (left) and Silicon (right)

change made in this figure was to correct the placement of the nitrided layer, since N_2, NO, N_2O, and NH_3 (Deshpande's claims 7,8,11,12,13,) cannot leave a layer on the semiconductor themselves, nor when used in combination with and inert gas (Deshpande's claims 9, 10, 14). So nitridation species must be acting in combination with the semiconductor substrate. Thus most or all of the effect of the nitridation step must be below the semiconductor surface.

- It is important to note that Deshpande makes no claim to the **deposition** of silicon nitride as his figures may mislead. In fact, Deshpande makes no claim to any added silicon at this step. The silicon in the nitrided layer over the silicon substrate comes from the substrate itself.
- The new layer that is formed in the GaAs case does not contain any silicon because the substrate must provide such silicon, and the GaAs substrate has no significant silicon (only impurity levels at best). So it would be incorrect to state that Deshpande's invention claims a layer of silicon nitride as a trench liner. It actually claims a layer of nitrided substrate semiconductor, which happens to be silicon nitride only in the case of a silicon substrate.
- Note that at this point the GaAs surface is likely to be permanently damaged with nitrogen, and certainly not have any anneal cap in place.
- In the case where NO or N_20 (Deshpande's claim 8) is used for the nitrogen-containing atmosphere, the damaged GaAs layer will include oxygen as well as nitrogen contamination.

- In the case where NH_3 is used for the nitrogen-containing atmosphere, the damaged GaAs layer will include hydrogen and nitrogen contamination.
- In the case where an inert gas is used in combination with the nitrogen-containing atmosphere (Deshpande's claim 9), the inert gas will also be a component of the contamination.
- In the case where an elevated temperature is used as part or all of the nitridation process (Deshpande's claims 11, 12), the depth of GaAs damage may be deeper, and missing some arsenic from its stoichiometry.
- In the case where a decoupled plasma nitridation process (Deshpande's claim 13) is used, the damage to the GaAs may be shallower.
- After applying all of the Deshpande claims applicable to this step and previous steps, individually or in combination, what we are left with on the GaAs wafer is not only a structure missing the anneal cap layer, but also a damaged semiconductor contaminated with nitrogen and possibly other elements. The purpose of the anneal cap layer is to protect the GaAs surface from damage when undergoing a subsequent high temperature step. This nitridation step has done the opposite by damaging the crystal in-situ.

- The next step, illustrated by Deshpande's Fig. 3E, is mostly replicated by figure 3 below. While this is the next logical step in the case for the silicon wafer, this step pre-

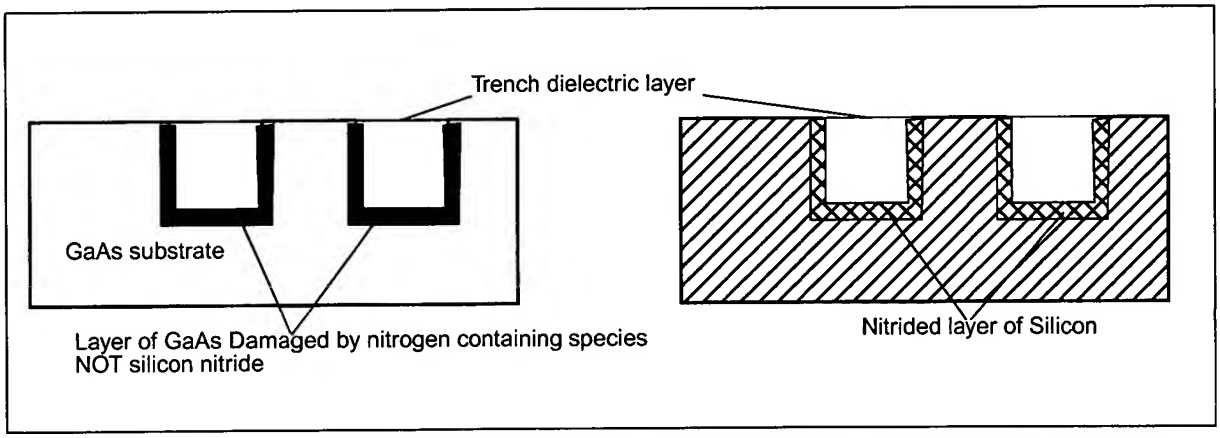

Figure 3: Structure views of Deshpande's process after planarization step on a GaAs wafer (left) and Silicon wafer (right)

cludes any chance for fixing the damage in the GaAs semiconductor.

- The purpose of the anneal cap on GaAs is to protect the GaAs crystal from damage during an anneal (high temperature) step. In some rare cases, an anneal cap may be avoided by using an arsenic over-pressure during anneal. By placing the trench dielectric layer immediately over the damaged semiconductor caused by the nitridation step, the surface will be forced to lose significant arsenic during anneal regardless of any overpressure used during an anneal step. This is true for any of the trench dielectric materials listed in Deshpande's detailed description: Conventional SiO_2, TEOS oxide, and HDP oxide.

- Even if the nitridation step were skipped, and the GaAs was not damaged yet, the inclusion of this oxide deposition step will result in the semiconductor being damaged. Since silicon oxide compounds do not act as stoichiometry preserving anneal caps, their direct interface with semiconductor cannot be considered compatible with GaAs.

- Deshpande's claims 1 and 21 imply the proceeding steps are to be followed by conventional CMOS processing using thermal oxidation. This is confirmed in the Background of the invention, the summary of the invention, and detailed description sections of the application. Figure 4 below shows the effect of the necessary thermal

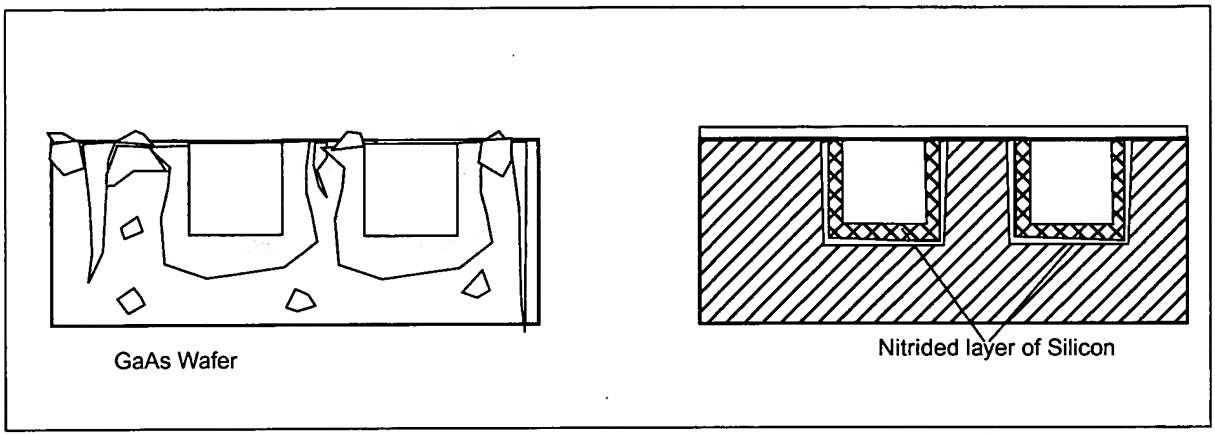

Figure 4: Comparing GaAs wafer (left) to silicon wafer (right) after thermal oxidation step

oxidation steps on both the III-V semiconductor structure and the silicon based structure.

- On the silicon wafer, the nitrided layer of silicon effectively reduces the amount of silicon that gets oxidized below it. This reduces the resulting stress on the edge of the isolation structure. The attempted thermal oxidation of the GaAs wafer is a disaster. The high temperature used in the thermal oxidation step in combination with the oxygen-containing ambient not only forms unstable gallium and arsenic oxides, but also allows significant arsenic to escape from the wafer, coating the inside of the equipment used for the process step. Such significant loss of arsenic breaks-down the crystal in such a way that large pits are left in the semiconductor surface.
- Thus a conventional CMOS process is incompatible with GaAs wafers, so an invention that reduces the amount of oxidation along the edge of an isolation structure during a gate thermal oxidation does not apply to GaAs.

- So in review, Deshpande in no way discloses a structure providing anneal cap/ion implant mask, and shallow trench isolation features for III-V devices comprising a trench etched into the semiconductor, a combination anneal cap/CMP stop layer, and a dielectric trench fill layer, with significant topography reduction compared to the traditional dielectric structure because:

- No silicon nitride layer is **deposited** in the Deshpande invention. The nitridation step not only does not protect the GaAs surface as an anneal cap, it outright damages the GaAs surface.
- The layer left by the nitridation of the GaAs in no way may act as a CMP stop layer because it adds nothing on top of the area to be protected during such a process.
- The problem Deshpande is fixing doesn't even apply to GaAs processing.

in re claims 2, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is GaAs (section [0038]).

Deshpande included the symbol "GaAs" in his claims, but as explained above, a structure resulting from his invention is of no use in GaAs processing.

In re claims 3, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is InP (section [00038]).

InP, being a binary semiconductor, has largely the same issues as GaAs. Deshpande included the symbol "InP" in his claims, but as explained in the response to claim 1 above, a structure resulting from his invention is of no use in InP processing.

In re claim 4, as best understood, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is GaAs with over-layers of other semiconductors specific to the devices fabricated [footnoted: As described in sections [0069-0071]. the device will be used in combination with various PFET and NFET devices, which will comprise over-layers of semiconductor, such as gate polysilicon layer, as a gate polysilicon layer, as is well known in the art.]

As is well known in the art of semiconductor processing of epitaxially grown materials, the term "over-layers" refers to subsequent layers of semiconductor epitaxially grown on a semiconductor substrate. Processing in a fabrication facility may start with either wafers of a single substrate material or semiconductor substrates with different semiconductor layers grown on top. This claim refers to the starting material in such a process. The starting material may be either a single semiconductor type with a single doping type, or several different layers of epitaxially grown semiconductors with various doping types and levels. "Over-layers" does not refer to the processing done after the invention is fabricated as indicated by the response above.

In re claim 5, as best understood, Deshpande discloses the device of claim 1, wherein said III-V semiconductor is InP with over-layers of other semiconductors specific to the devices fabricated [footnoted: As described in sections [0069-0071], the device will be used in combination with various PFET and NFET devices, which will comprise over-layers of semiconductor, such as gate polysilicon layer, as is well known in the art.]

As in the case of GaAs above, starting material in an InP semiconductor product manufacturing facility may be either bulk InP substrate wafers, or wafers with epitaxial layers grown on top. This claim was intended to include both cases of starting material

In re claim 8, Deshpande discloses the device of claim 1, wherein said dielectric trench fill layer is silicon dioxide (section [0061].

This claim does not stand alone it is dependent on claim 1 which, as shown above is a completely different invention from Deshpande's.

Claim Rejections - 35 USC § 103

5. The following is a quotation of the 35 U.S.C 103(a) which forms the basis for all obviousness rejections set forth in the Office action: [quote deleted].

6. Claims 6 and 7 are rejected under 35 U.S.C 103(a) as being unpatentable over Deshpande et al. as applied to claim 1 above, and further in view of Ohta (US 2004/0126990 A1).

In re claim 6, Deshpande discloses the device of claim 1, but does not expressly disclose the silicon nitride layer being in the range of 100 to 3000 angstroms. Ohta discloses a silicon nitride liner having a thickness of 20 to 40 nm, which equates to 200 to 400 angstroms. It would have been obvious for one skilled in the art at the time of the invention to use a thicker liner layer as disclosed by Ohta for the device of Deshpande for the purpose, for example of enhancing FET characteristics, such as increased drain current, by generating greater tensile stress in the silicon nitride layer (Ohta; section s 0032; 0045, 0056]).

Deshpande's method does not disclose a silicon nitride layer on III-V semiconductors, it discloses a nitrided layer of the underlying semiconductor. Only on silicon would it be silicon nitride. On GaAs, it would be $GaAs_xN_y$. As mentioned in the response to claim 1 objections above, the $GaAs_xN_y$ not only implies damage to the GaAs surface that allowed it's creation, but it also would not act as an anneal cap to the underlying GaAs.

Ohta teaches a layer of thermally oxidized silicon (layer 7 in Fig.s 2B, 2C-J, 3B, 4A-D, 5A-J, 6A-D, 7A-D, 8A-D, paragraph [0051],) below the nitride layer. Since:

- Thermally oxidizing III-V semiconductors such as GaAs does not yield thermally oxidized silicon since there is no source of silicon in this process;
- Exposing III-V semiconductors such as GaAs to processes intended for thermally oxidizing silicon will destroy the semiconductor;
- Depositing SiO_2 directly on III-V semiconductors such as GaAs will not allow for any capping layer to protect the GaAs during subsequent anneal cycles, and will preclude the use of an arsenic overpressure during such anneals;

Ohta's structure is not only different from the present invention, it is also incompatible with GaAs and other III-V semiconductors. As in the case of Deshpande's invention, Ohta's invention is further incompatible with III-V semiconductors because of the associated conventional CMOS process steps it was clearly meant for. The most significant of these is the thermal oxidation of the semiconductor used for the gate oxide.

In re claim 7, Deshpande discloses the device of claim 1,. Ohta discloses a silicon nitride liner having a thickness of 24 to 40nm, which equates to 2 to 4 percent of the trench depth. Deshpande discloses the claimed invention wherein the trench depth is in the range of 1μm (1000nm), section [0047], but does not expressly disclose the silicon nitride layer having a thickness of 5 to 25 percent of the trench depth. It would have been

obvious to one having ordinary skill in the art at the time the invention was made to increase the thickness of the nitride liner since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller 105 USPQ 233. To Do so would improve the FET characteristics, such as drain current, as disclosed by Ohta (sections [0032, 0045, 0056]).

Deshpande does not disclose a silicon nitride layer on GaAs or other III-V semiconductors. He discloses a $GaAs_xN_y$ layer on GaAs, or in general, a $(III)(V)_xN_y$ layer on III-V semiconductors. While Ohta specifically calls out a silicon nitride layer, the silicon nitride layer is deposited on a silicon dioxide layer (layer 7 in Fig.s 2B, 2C-J, 3B, 4A-D, 5A-J, 6A-D, 7A-D, 8A-D). One skilled in the art notices that Ohta uses the word "trench" with at least three different definitions in his application. In the first use, "trench" is used to describe a thermally oxidized hole in the silicon semiconductor substrate (see Ohta's claims 1,13,14, 15, 19, 20, 24 and paragraphs [0029], [0030], [0031], [0049], [0053], [0054], [0055], [0090], [0095]). However, when Ohta specifically refers to component 6 in the figures, he uses "trench" to refer to simply the hole etched in the semiconductor (paragraphs [0015], [0016], [0053], [0054], [0055], [0090]). Ohta also uses the word "trench" to describe a hole etched in the silicon lined with thermal oxide plus other layers (paragraphs [0061], [0066], [0070], [0095], [0096], [0110], [0111], [0118], [0129]). Nowhere does Ohta prescribe putting silicon nitride directly on the semiconductor. Even if he did, subsequent steps, necessary to the CMOS process his invention is associated with, would cause oxidation at the interface. So the final structure cannot possibly have silicon nitride directly on the silicon substrate surface.

Thus whether the thicknesses of nitride Ohta discloses are similar to the present invention is irrelevant since neither the structure nor the application are the same. Ohta's structure is one that is compatible with silicon, not GaAs or other III-V semiconductors, and the invention is used to fix a problem in CMOS, not one that exists in III-V device technologies.

Response to Arguments

1. Applicant's arguments filed 06/06/05 have been fully considered but they are not persuasive.

a. First, applicant argues that Deshpande in Fig 3E does "not illustrate the final structure formed in fabricating the device..." However, as noted in the Deshpande reference under the "Brief Description of the Drawings," Deshpande discloses that Fig. 3E is the final drawing of the first embodiment of the invention. This can also be seen from paragraph [0064]-[0065], where Deshpande stops describing the Fig. 3 embodiments, and begins to describe Fig. 4 and beyond.

To one skilled in the art it is obvious that Deshpande's invention applies only to steps early in the fabrication of a semiconductor part, and in no way represents the final state of the structure. This can also be clearly seen by the first two words of the only independent claim 1, "A method". Given this is a method invention, Deshpande evidently has no compelling need to show the details of what things look like after his method has concluded. The right side of Figure 4 above shows this type of detail for the unexperienced

reader. Contrary to the examiner's assertion, Deshpande does make it clear that further processing will be necessary after what is shown in Fig. 3E in paragraphs [0062]-[0063], then again in paragraph [0066], then again in paragraphs [0070]-[0071]. The words, "gate dielectric formation" tell of the thermal oxidation yet to come that will oxidize the silicon surfaces, both on the surface and embedded. This thermal oxidation step will cause disastrous results on III-V semiconductors as illustrated on the left side of figure 4 above.

It must also be noted that Deshpande's figures calling the nitrided layer, "silicon nitride" only apply to a silicon substrate, since a different compound will exist for that "layer" in III-V semiconductors.

b. Second, applicant asserts that there is an additional thermal oxidation process that much [must] *be performed for the device of Deshpande that will produce an additional layer not essential to the device of the instant application.*

i. To satisfy 35 USC 102, a prior art reference may consist or [of] *more components that a claimed invention, so long as the prior art contains all of the essential elements of the claimed invention in a consistent manner. For example, if a claim asserts a three-layer insulation stack of A/B/C, and the prior art teaches a four-layer stack of A/B/C/D, then the prior art duly anticipates the claim, even though there is an additional layer. Such is the case here. Applicant is asserting that the disclosure of Deshpande discloses more than is claimed. That fact is not a bar to the anticipation determination under 35 USC 102.*

Our explanation of the additional thermal oxidation step was not intended to merely tally a "count" of layers. The purpose was to describe the actual structure that resulted from Deshpande's method. This demonstrated the structure was not only different from the present invention, but also that such a structure was not compatible with III-V semiconductors.

The Examiner states that an additional oxide layer is "not essential to the device of the instant application." Since this statement would imply the thermal SiO2 layer essential to Deshpande's invention is optional to the present structure on III-V semiconductors, the statement is false. As stated above, both the existence of the silicon dioxide on the III-V semiconductor surface, and specifically, the process to form thermal oxide on silicon, would cause destruction to the III-V semiconductor.

ii. Second, applicant does not establish where in Deshpande this thermal oxidation layer is disclosed and the underlying structure differs from that claimed.

To one skilled in the art, it is obvious the thermal oxidation layer must exist for two reasons:

- The whole point of Deshpande's invention is to remedy a side-effect of such an oxidation.
- All conventional CMOS, which Deshpande's invention clearly is made for, uses such layers. This statement cannot be understated. At the beginning of the integrated circuit industry, silicon was chosen over germanium largely because of silicon's stable native oxide. Even now, the only materials that have ever been in contact with silicon on any technology that has ever gone into real manufacturing is thermal SiO_2, or in

the last decade, thermally oxidized nitrided silicon called oxynitride. The silicon semiconductor industry clearly does not consider SiO_2 to be an optional layer that could easily be removed as implied by the patent examiner. The latest road-map for the silicon semiconductor industry calls for the insertion of a so called "High K" gate dielectric into the 45 nm generation. This would enter into high volume manufacturing in 2007 or 2008, but already many pundits have speculated that the industry is not ready for this insertion at the 45 nm node. In fact the industry is extremely cautious and fearful about anything other than thermal SiO2 or oxynitride being in contact with silicon.

Besides the obviousness to one skilled in the art, Deshpande explicitly states the existence of such layers in paragraphs [0062]-[0063], then again in paragraph [0066], then again in paragraphs [0070]-[0071]. The words "gate dielectric formation" tell of the thermal oxidation yet to come that will oxidize the silicon surfaces, both on the surface and embedded.

c. Third, applicant argues that Deshpande is using his structure for a different use than the claimed invention. Specifically, that Deshpande is using the structure for the minimization of the bird's beak effect. Intended use descriptions do not make or break patentability determinations. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art. Therefore, if the prior art uses the disclosed device for a purpose not enunciated or contemplated by the applicant, such as distinction does not eliminate the prior art from anticipation or obviousness consideration.

i. Additionally, the language of applicant, "a combination anneal cap/CMP stop layer" is intended use language that does not work to further define the claimed structure over the prior art. As claimed, applicant's structure comprises a III-V substrate, a trench liner layer, and a fill layer. The same is disclosed by Deshpande.

Mentioning the distinct differences is use between the two different inventions was meant for further clarification of the form of the invention itself rather than to be the exclusive distinction. Not only is Deshpande's invention not the same as the present invention, but Deshpande's invention wouldn't even work for the designated purpose of our invention. The USPTO has made it clear that a patent application must be enabling. The fact that Deshpande has disclosed a method that results in a structure with a trench liner layer and a fill layer on silicon, is by no means enabling on GaAs or other III-V semiconductors. Deshpande's invention wouldn't even result in a structure with a trench liner on GaAs.

d. Lastly, applicant argues that Deshpande does not disclose an anneal cap or that the thermal oxide layer grown from the semiconductor substrate is likely to be a poor anneal cap. Whether applicant characterizes the anneal cap of Deshpande as good or poor does not obviate the fact that Deshpande disclose an analogous structure to that of the claimed invention.

The examiner has incorrectly interpreted the use of the words "poor anneal cap". In our response, the use of "poor" is analogous to the use of "poor" in the sentence, "A fishnet is a poor bullet proof vest". For clarity, in the above discussion we did not use the words, "poor anneal cap", but instead substituted phrases similar to, "would not act as an anneal

cap". Because Deshpande has indicated no layer that may act as an anneal cap he has not disclosed an analogous structure to that of the claimed invention. He has only disclosed a method for reducing unwanted oxidation in a silicon MOS structure.